

CLAIMS:

What is claimed is:

- 1 1. An apparatus comprising:  
 2 a processor handling an I/O request in an I/O operation;  
 3 main storage controlled by the processor for storing data;  
 4 one or more I/O devices for sending data to or receiving data from said main storage;  
 5 a vector mechanism operable to register I/O requests by said devices to send or receive  
 6 data from said main storage;  
 7 a dispatcher operable to poll said vector mechanism to determine if there is an outstanding  
 8 I/O request; and  
 9 an override bit having a first condition when an immediate interrupt is to be sent to said  
 10 processor for handling an I/O request from said I/O device(s), and a second condition when said  
 11 dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said  
 12 override bit being set to its first condition or reset to its second condition by said processor.
- 1 2. The apparatus of claim 1 further comprising a Target Delay Interval (TDI) register  
 2 containing a TDI value for determining when the vector mechanism should not be polled by said  
 3 dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first  
 4 condition, overrides said TDI value and drives an immediate interrupt to said processor.
- 1 3. The apparatus of claim 1 wherein said main storage is divided into multiple partitions, with  
 2 each partition having a vector mechanism operable to register I/O requests by said devices to send  
 3 or receive data from that partition of main storage, each partition having an associated override bit  
 4 for that partition, and said processor is a hypervisor for setting the override bit for that partition  
 5 when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for  
 6 that partition.

1 4. The apparatus of claim 3 further comprising one or more central processing units (CPUs)  
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the  
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 5. The apparatus of claim 1 wherein said override bit is reset to its second condition after an  
2 interrupt is handled by said processor.

1 6. The apparatus of claim 5 wherein said override bit is reset to its second condition after said  
2 dispatcher polls said vector mechanism, said resetting of said override bit to its second condition  
3 upon the first to occur of said interrupt handling or said dispatcher polling.

1 7. An apparatus controlling the transfer of data in a data processing system having a  
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor  
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main  
4 storage, said apparatus comprising:

5 a vector mechanism operable to register I/O requests by said devices to send or receive  
6 data from said main storage;

7 a dispatcher operable to poll said vector mechanism to determine if there is an outstanding  
8 I/O request;

9 an override bit having a first condition when an immediate interrupt is to be sent to said  
10 processor for handling an I/O request from said I/O device(s), and a second condition when said  
11 dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said  
12 override bit being set to its first condition or reset to its second condition by said processor.

1 8. The apparatus of claim 7 further comprising a Target Delay Interval (TDI) register  
2 containing a TDI value for determining when the vector mechanism should not be polled by said  
3 dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first  
4 condition, overrides said TDI value and drives an immediate interrupt to said processor.

1 9. The apparatus of claim 7 wherein said main storage is divided into multiple partitions, with  
2 each partition having a vector mechanism operable to register I/O requests by said devices to send  
3 or receive data from that partition of main storage, each partition having an associated override bit  
4 for that partition, and said processor is a hypervisor for setting the override bit for that partition  
5 when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for  
6 that partition.

1 10. The apparatus of claim 9 further comprising one or more central processing units (CPUs)  
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the  
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 11. The apparatus of claim 7 wherein said override bit is reset to its second condition after an  
2 interrupt is handled by said processor.

1 12. The apparatus of claim 11 wherein said override bit is reset to its second condition after  
2 said dispatcher polls said vector mechanism, said resetting of said override bit to its second  
3 condition upon the first to occur of said interrupt handling or said dispatcher polling.

1 13. A method for controlling the transfer of data in a data processing system having a  
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor  
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main  
4 storage, said method comprising:  
5 registering in a vector mechanism, I/O requests by said devices to send or receive data  
6 from said main storage;  
7 polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O  
8 request; and  
9 sending an immediate interrupt to said processor when an override bit has a first condition  
10 for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector  
11 mechanism to determine if there is an outstanding I/O request when said override bit is in a second  
12 condition.